

# Project Name: NSBW140X

Platform : Braswell

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- 28. VCC Switch
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- 30. USB HUB
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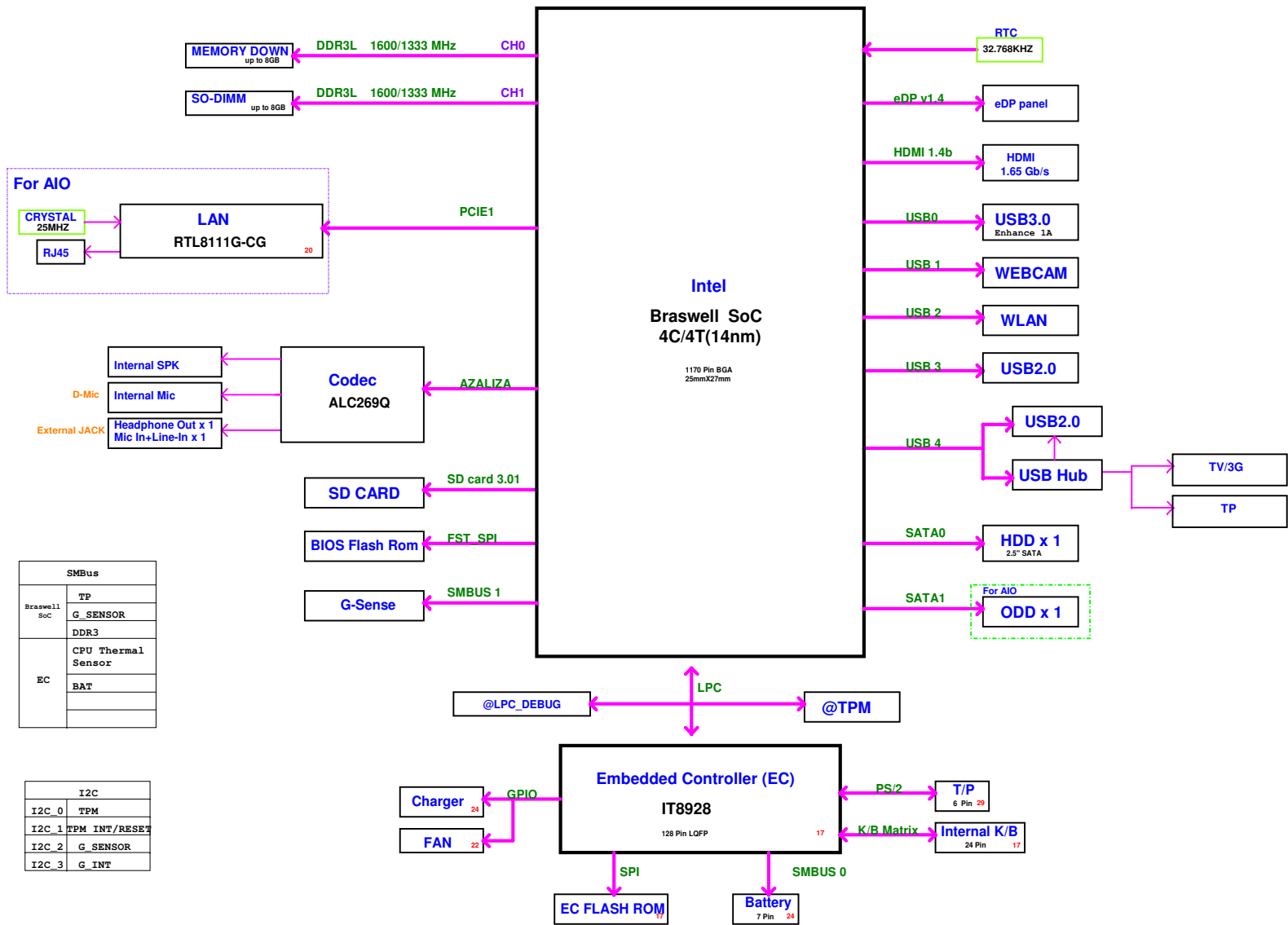
## M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

## Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

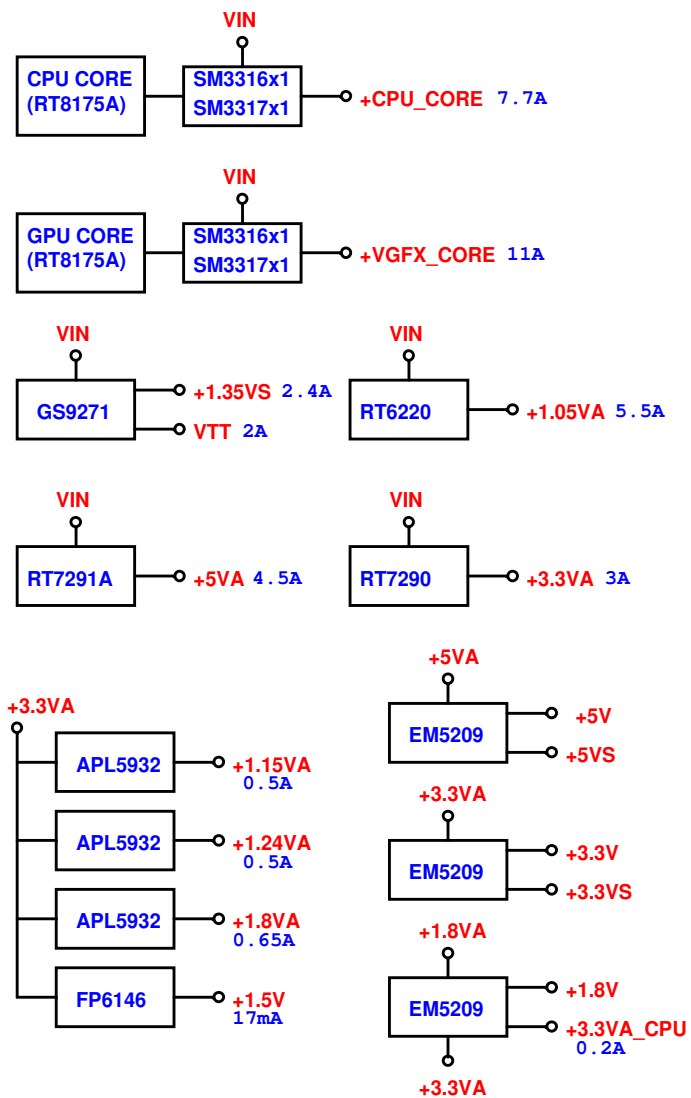
NSBW140X BLOCK DIAGRAM



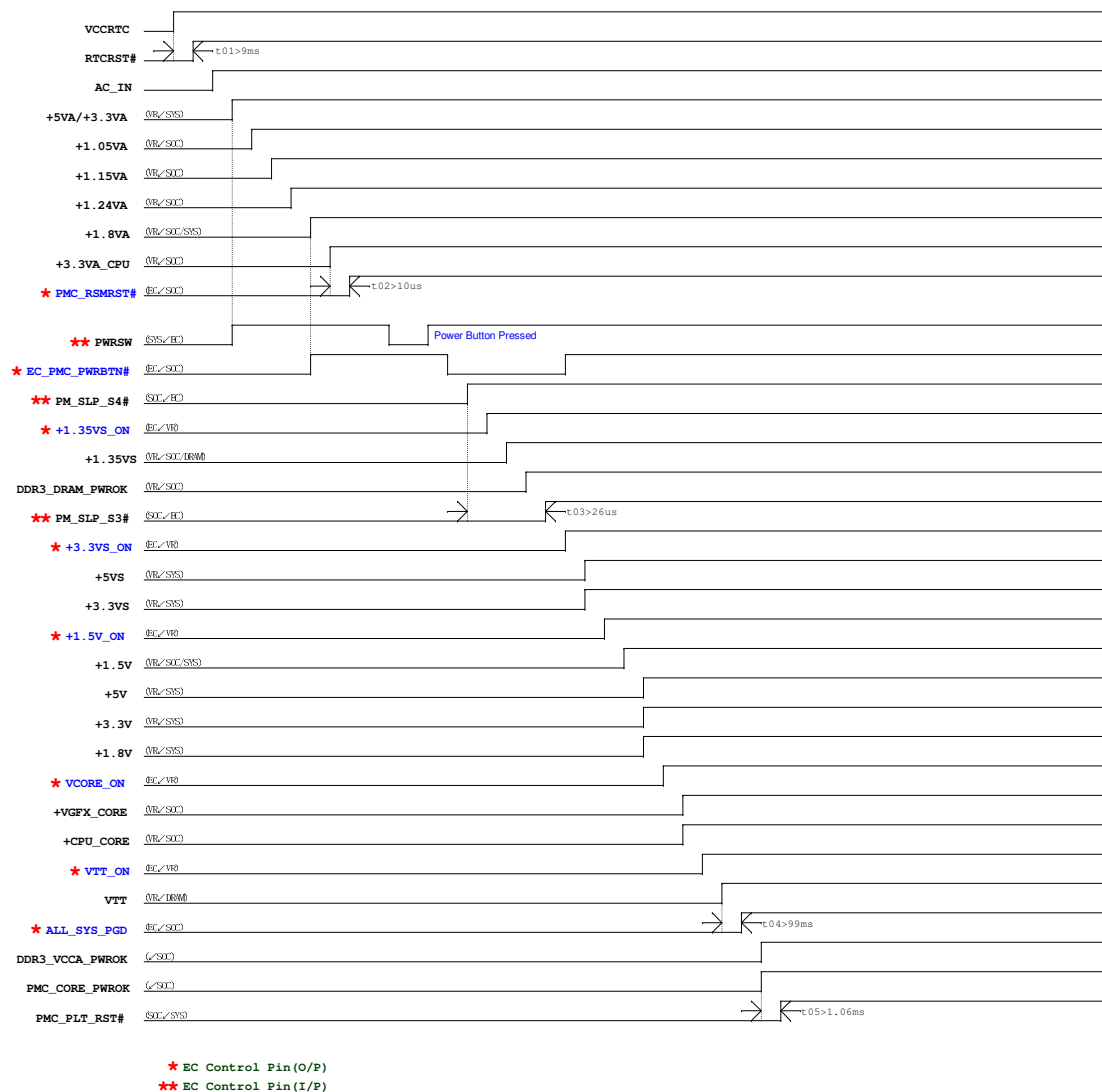
SMBus	
Braswell SoC	TP
	G_SENSOR
	DDR3
EC	CPU Thermal Sensor
	BAT

I2C	
I2C_0	TPM
I2C_1	TPM INT/RESET
I2C_2	G_SENSOR
I2C_3	G_INT

# POWER BLOCK DIAGRAM



## Power On Sequence



Input Power	Voltage	Current	Power Rail	Voltage	Current
VIN	12-19V	4.1A	+CPU_CORE	VID	7.7A
			+VGFX_CORE	VID	11.0A
			+1.35VS	1.35V	8.0A
			VTT	0.675V	2.0A
			+1.05VA	1.05V	5.5A
			+5VA	5.0V	5.5A
			+3.3VA	3.3V	3.0A

Input Power	Voltage	Current	Power Rail	Voltage	Current
+3.3VA	3.3V	3.0A	+3.3VA_CPU	3.3V	0.2A
			+1.15VA	1.15V	0.5A
			+1.24VA	1.24V	0.5A
			+1.08VA	1.8V	0.65A
			+1.5V	1.5V	0.02A
			+3.3V/+3.3VS	3.3V	1.5A

Input Power	Voltage	Current	Power Rail	Voltage	Current
+5VA	5.0V	5.5A	+5V/+5VS	5V	5.5A

## ITE8928

## Default

	GPIO	Pull/Mode	DSN LEVEL	EC LEVEL	IC LEVEL	Comment
GPA0	PID_1_CHG_R_LED	UP/GPO	3.3VA	3.3V		Reserved
GPA1	PID_2_PWR_LED	UP/GPO	3.3VA	3.3V		Reserved
GPA2	BTL_BEEP	/GPO		3.3V	3.3V	Reserved
GPA3	Fast_Charge	/GPO	3.3V	3.3V	3.3V	
GPA4	+1.05VA_ON	UP / GPO	3.3VA	3.3V	>1.25V	Reserved
GPA5	SENBAT_V	/ GPO	3.3V	3.3V	For NMOS	
GPA6	PMC_RSMRST#	Dn / GPI	3.3V	3.3V	3.3V	
GPA7	+1.35VS_ON	/ GPO	3.3V	3.3V	>1.25V	
GPB0	WLAN_HOST_WAKE	/ GPI	3.3V	3.3V	3.3V	Reserved
GPB1	WLAN_SUSPEND	/ GPO	3.3V	3.3V	3.3V	Reserved
GPB2	WEBCAM_ON	/ GPO	3.3V	3.3V	3.3V	
GPB3	BAT_SMBCLK1	UP/GPIO	3.3VA	1.8VA		
GPB4	BAT_SMBDAT1	UP/GPIO	3.3VA	1.8VA		
GPB5	SOC_BL_EN	/ GPI	1.8VA	1.8/3.3VA	MAX 5.0V	Reserved
GPB6	+3.3V_EC	UP / GPI	3.3VA	1.8/3.3VA	3.3V	
GPB7	SAFTY_PROTECT	Dn / GPO	3.3V	3.3V	For NMOS	
GPC0	3G_Power_ON_EC	/ GPO	3.3VA	1.8/3.3VA	3.3V	Reserved
GPC1	SMB_CLK_EC	UP / GPIO	3.3VA	1.8/3.3VA	3.3V	
GPC2	SMB_DATA_EC	UP / GPIO	3.3VA	1.8/3.3VA	3.3V	
GPC3	PWRBTN1#	UP / GPI	3.3VS	3.3V	3.3V	Reserved
GPC4	PANEL_DETECT 2	UP / GPI	3.3VA	3.3V	3.3V	
GPC5	CHG_HI_VOLT#	/ GPO	3.3V	3.3V	For NMOS	
GPC6	PANEL_3.3V_ON	UP /GPO	3.3V	3.3V	For NMOS	
GPC7	VTT_ON	/ GPO	3.3V	1.8/3.3VA	>1.25V	
GPD0	ADAP_IN	Dn / GPI	3.3V	1.8/3.3VA	For NMOS	
GPD1	EC_PMC_PWRBTN#	UP / GPO	1.8VA	1.8/3.3VA	1.8V	
GPD2	PLT_RST#	UP / GPI	3.3V	1.8/3.3VA	3.3V	
GPD3	SMC_WAKE_SCI#	Up / GPO	1.8VA	1.8/3.3VA	1.8V	Reserved
GPD4	EC_EXTSMI#	UP / GPO	1.8VA	1.8/3.3VA	1.8V	
GPD5	NC					
GPD6	+1.5V_ON	/ GPO	3.3V	3.3V	3.3V	
GPD7	PWR_USB#	UP/ GPO	3.3VA	3.3V	3.3V	
GPE0	LID#	UP / GPI	3.3VA	1.8/3.3VA	3.3V	
GPE1	AMP_MUTE#	/ GPO	3.3V	3.3V	3.3V	
GPE2	ALL_SYS_PGD	/ GPO	3.3V	3.3V	For NMOS	
GPE3	VCORE_ON	/ GPO	3.3V	3.3V	3.3V	
GPE4	PWRSW	UP / GPI	3.3VA	3.3V	3.3V	
GPE5	LVDS_VIN	/ GPO	3.3V	3.3V	For NMOS	
GPE6	3G_SIM_DET_EC	/ GPI	3.3V	1.8/3.3VA	3.3V	Reserved
GPE7	PMC_SLP_S0IX#_R	/ GPI	3.3V	1.8/3.3VA	3.3V	Reserved
GPF0	PANEL_VCC	Dn / GPO	3.3V	3.3V	3.3V	Reserved
GPF1	TXE_DISABLE	/ GPO	3.3V	3.3V	For NMOS	
GPF2	3G_Reset_EC	/ GPO	3.3V	1.8/3.3VA	3.3V	Reserved
GPF3	WLAN_ON	/ GPO	3.3V	1.8/3.3VA	For NMOS	
GPF4	TP_CLK	UP / GPIO	3.3V	1.8/3.3VA	3.3V	
GPF5	TP_DATA	UP / GPIO	3.3V	1.8/3.3VA	3.3V	
GPF6	PM_SLP_S3#	UP / GPIO	3.3VA	1.8/3.3VA	connect to level shifter	
GPF7	PM_SLP_S4#	UP / GPI	3.3VA	1.8/3.3VA	connect to level shifter	
GPG0	NC					
GPG1	+3.3VS_ON	/GPO	3.3V	3.3V	3.3V	
GPG2	NC					
GPG3	SPI_CE#	/GPO		3.3V	3.3V	
GPG4	SPI_SI	/GPI		3.3V	3.3V	
GPG5	SPI_SO	/GPO		3.3V	3.3V	
GPG6	LAN_PW_EN	UP/GPO	3.3V	3.3V	For NMOS	
GPG7	SPI_CLK	/GPO		3.3V	3.3V	
GPH0	AUX_OFF	Dn/GPO	3.3VA	1.8/3.3VA	For NMOS	
GPH1	PID_3_RF_LED_ON#	/GPO	3.3VA	1.8/3.3VA	3.3V	
GPH2	EC_LCDVDD_EN	UP/GPO	1.8VA	1.8/3.3VA	1.8V	
GPH3	RST	/GPO	3.3V	3.3V	For NMOS	Reserved
GPH4	PLATFORM_ID1	UP/GPI/ID1	3.3VA	3.3V	3.3V	
GPH5	PLATFORM_ID2	UP/GPI/ID2	3.3VA	3.3V	3.3V	Reserved
GPH6	PLATFORM_ID3	Dn/GPI/ID3	3.3VA	3.3V	3.3V	
GPH7	NC					

	GPIO	Pull/Mode	LEVEL	EC LEVEL	IC LEVEL	Comment
GPI0	CPU_THERMAL_SENSE	UP/GPI/ADC	3.3V	3.3V	3.3V	
GPI1	PANEL_DETECT	UP/GPI	3.3VA	3.3V	3.3V	
GPI2	LAN_WAKE#	UP/GPI	3.3VS	3.3V	3.3V	EC Reserved
GPI3	PWRBTN2#	UP/GPI	3.3VS	3.3V	3.3V	Reserved
GPI4	BAT_I	/GPI/ADC	3.3V	3.3V	3.3V	Reserved
GPI5	BATT_TEMP	UP/GPI/ADC	3.3VA	3.3V	3.3V	
GPI6	ADAPTOR	Dn/GPI/ADC	3.3V	3.3V	3.3V	
GPI7	BAT_V	/GPI/ADC	3.3V	3.3V	3.3V	
GPJ0	EC_BL_ON	/GPO	3.3V	3.3V	<5V	
GPJ1	EC_PROCHOT	/GPO	3.3V	3.3V	For NMOS	
GPJ2	FAN_CTRL0	/GPO/DAC	3.3V	3.3V	3.3V	
GPJ3	WK_TH	/GPO/DAC	3.3V	3.3V	3.3V	
GPJ4	CHG_I	/GPO/DAC	3.3V	3.3V	3V	
GPJ5	SET_V	Dn/GPO/DAC	3.3V	3.3V	3.3V	
GPJ6	BATT_VA_OFF#	Dn/GPO	3.3V	3.3V	For NMOS	
GPJ7	3G_Module_ON_EC	/GPO	3.3V	3.3V	3.3V	Reserved
GPM0	LPC_AD0_EC	/GPIO	1.8V	1.8V	1.8V	
GPM1	LPC_AD1_EC	/GPIO	1.8V	1.8V	1.8V	
GPM2	LPC_AD2_EC	/GPIO	1.8V	1.8V	1.8V	
GPM3	LPC_AD3_EC	/GPIO	1.8V	1.8V	1.8V	
GPM4	CLK_EC_LPC	/GPI	1.8V	1.8V	1.8V	
GPM5	LPC_FRAME#	/GPI	1.8V	1.8V	1.8V	
GPM6	INT_SERIRQ	UP/GPIO	1.8VA	1.8V	1.8V	
GPM7						

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NSBW1401



eDP Logic Power EN

DDH1\_VDDEN

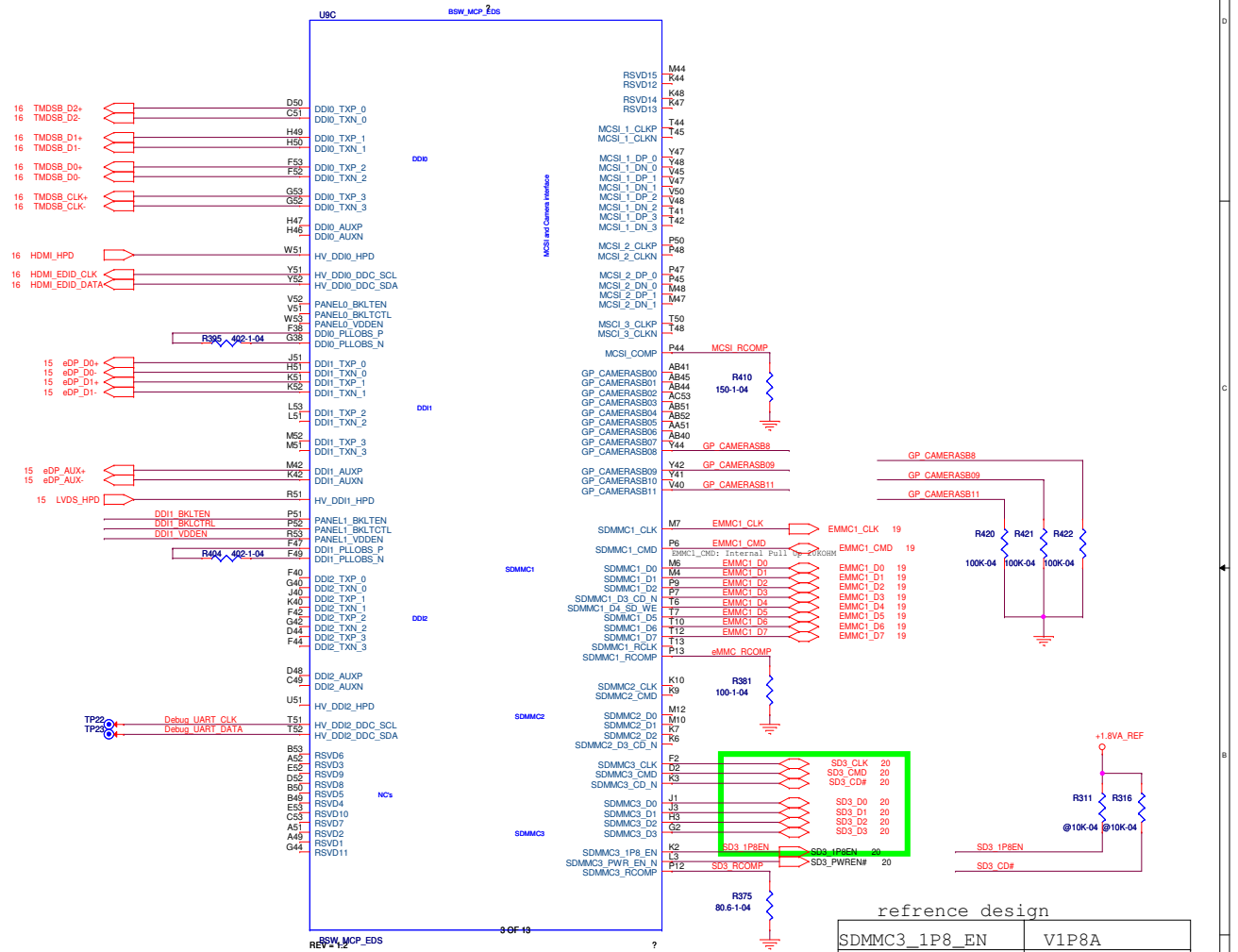
R415 1 2 0-04

R416 @100K-04

EC\_LCDVDD\_EN 17

**eDP BL Power EN**

The schematic shows a signal line labeled **DDH1\_BKL1EN** (pin 1) connected to the **SOC\_BL\_EN** pin (pin 17) of the SoC. The signal line is pulled up to **+1.8V\_REF** by resistor **R444** (10K-04) and pulled down to ground by resistor **R427** (100K-04). A label **R428 0-04** is also present near the signal line.

[illegible]

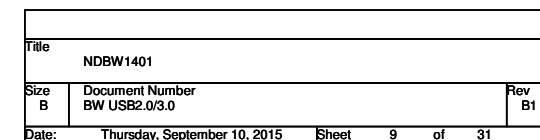
reference design	
SDMMC3_1P8_EN	V1P8A
SDMMC3_CD_N	V1P8A
SDMMC3_CLK	V3P3A/V1P8A
SDMMC3_CMD	V3P3A/V1P8A
SDMMC3_D0	V3P3A/V1P8A
SDMMC3_D1	V3P3A/V1P8A
SDMMC3_D2	V3P3A/V1P8A
SDMMC3_D3	V3P3A/V1P8A
SDMMC3_PWR_EN_N	V1P8A

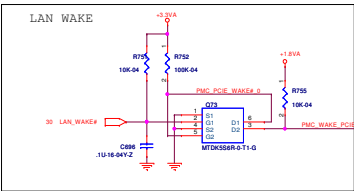
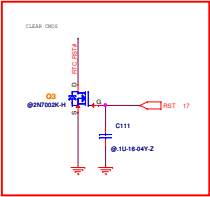
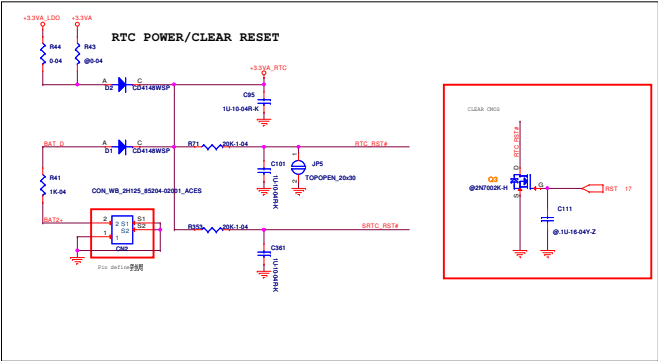
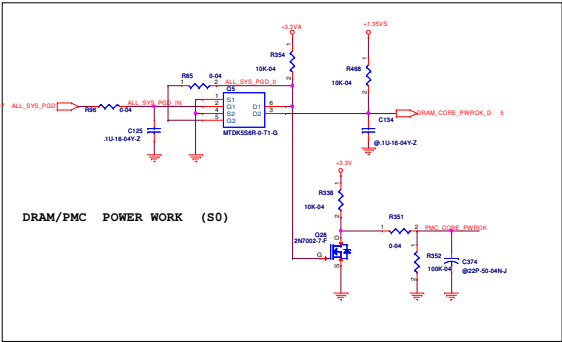
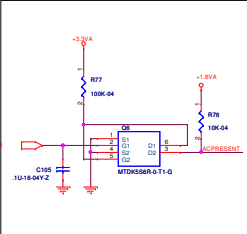
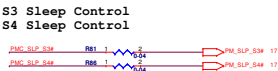
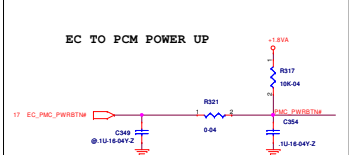
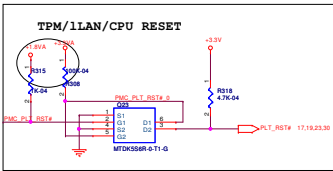
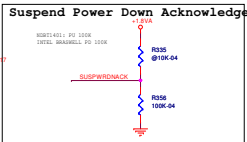
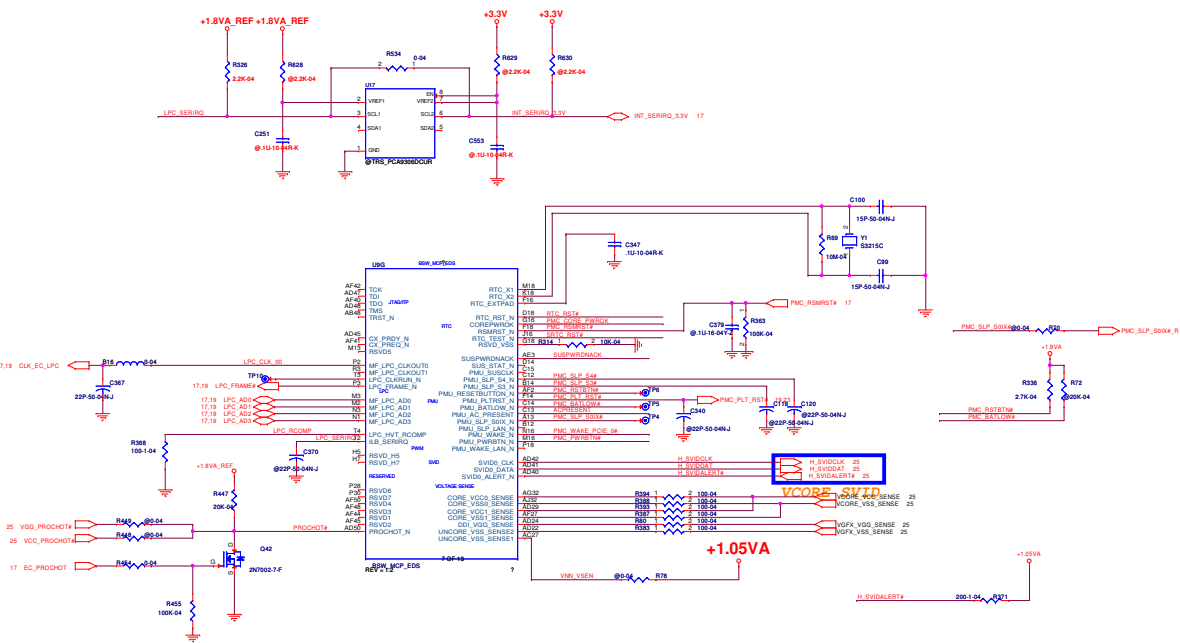






USB0	USB3.0/DEBUG
USB1	USB2.0
USB2	USB2.0
USB3	USB WLAN
USB4	USB HUB/ WEBCAM





**+CPU\_CORE MAX=6.4A**

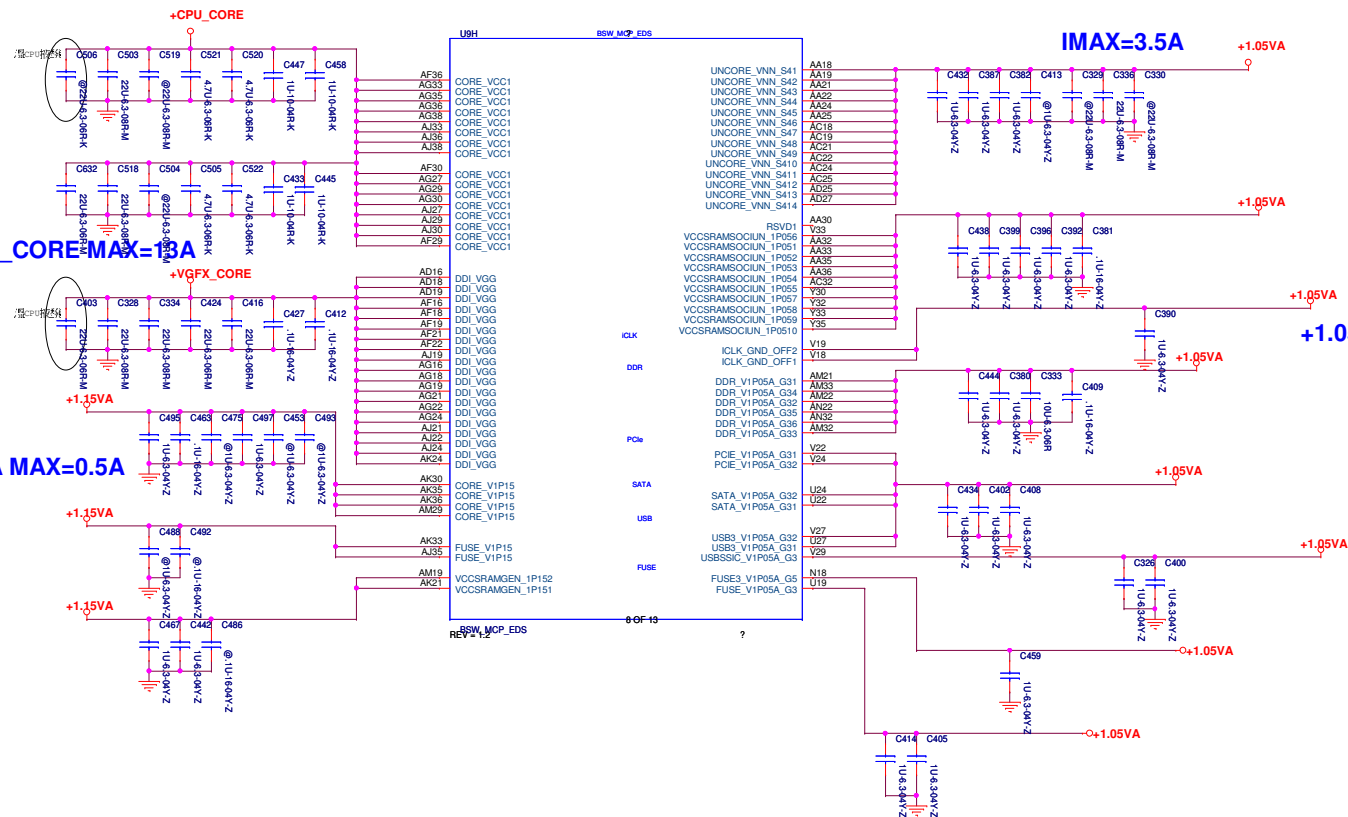
+CPU\_CORE

**+VGFX\_CORE MAX=13A**

+VGFX\_CORE

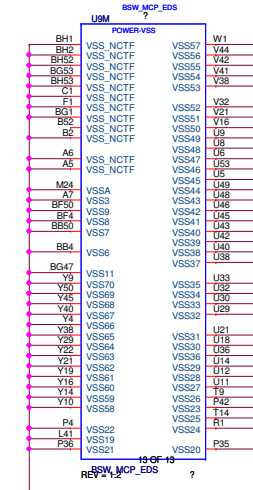
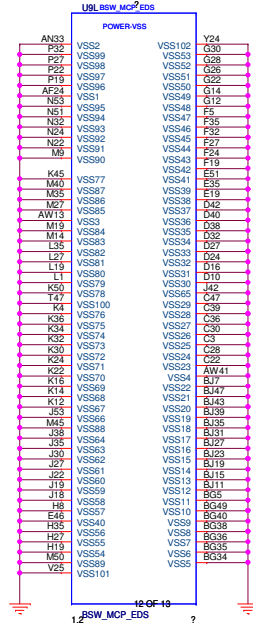
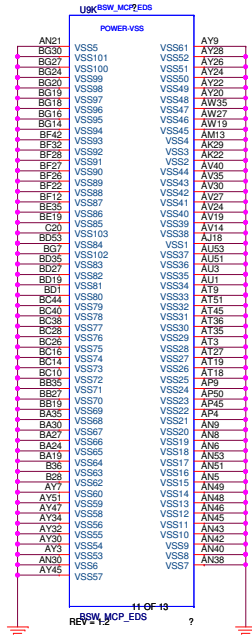
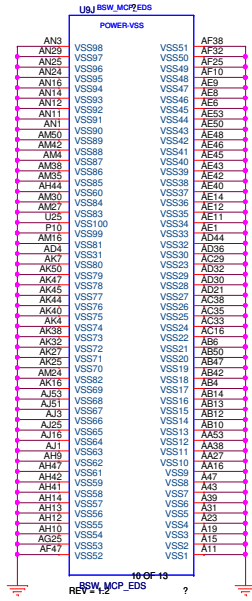
**+1.15VA MAX=0.5A**

**+1.05VA MAX=2A**



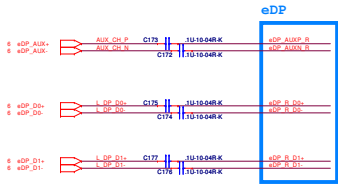
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C	BW POWER1			
Date:		Thursday, September 10, 2015	Sheet	11 of 31





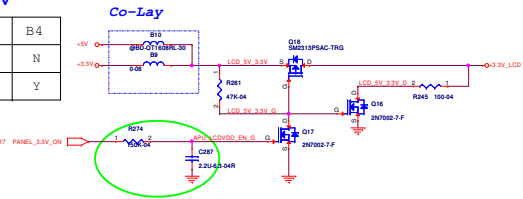


eDP

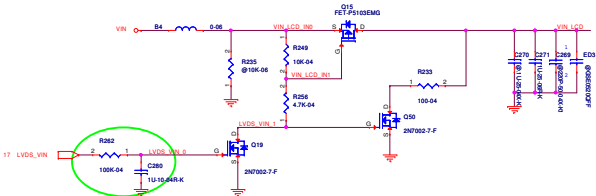


LCD 3.3V/5V

LCD_VDDIO	B3	B4
+5V	Y	N
+3.3V	N	Y

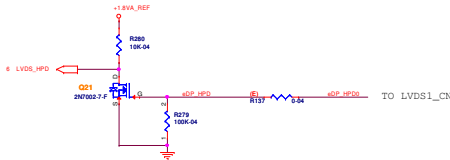


LCD 19V/BAT1+



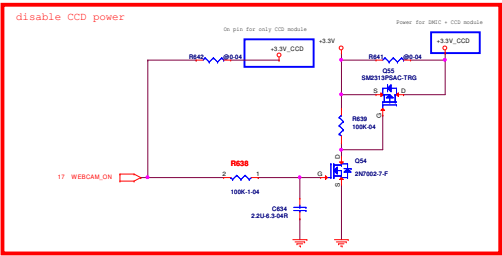
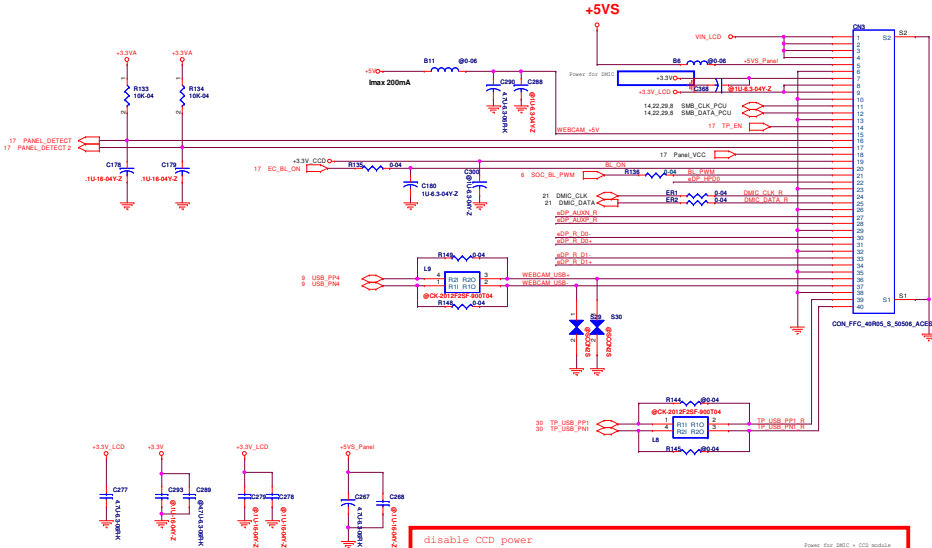
LCD HPD

LCD HPD	R183	R177
LVD5	Y	N
eDP	N	Y



Panel Connector

	High	Low
PANEL_DETECT1	1.4"	1.5"
PANEL_DETECT2	1.5"	1.6"

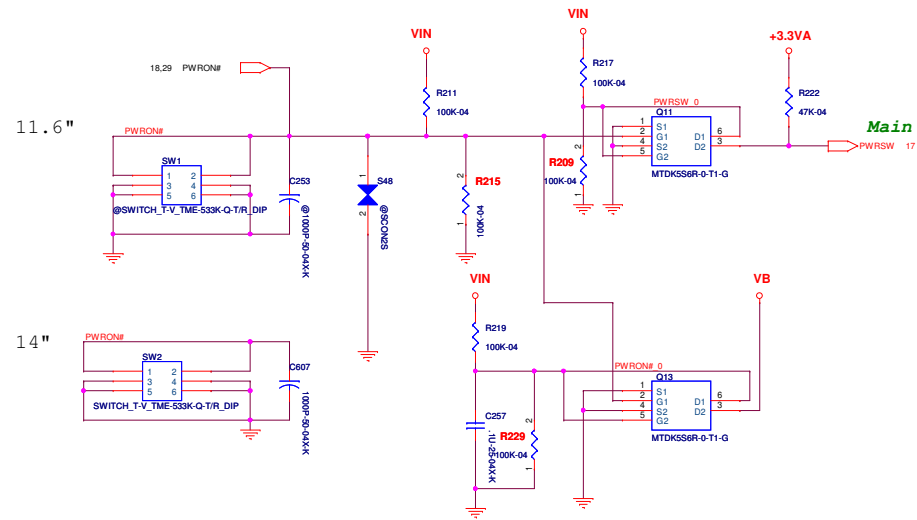




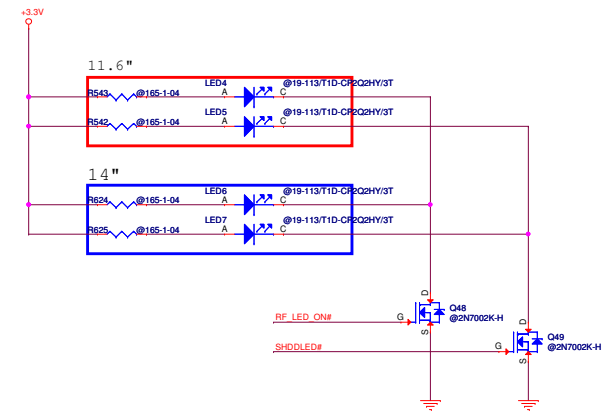




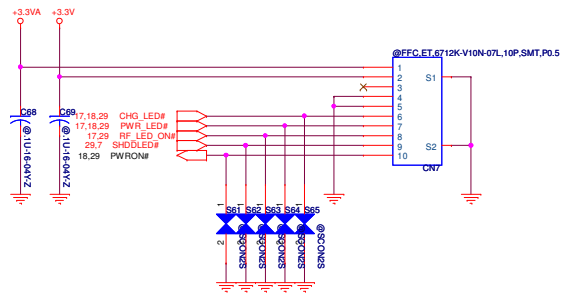
**PWR SW**



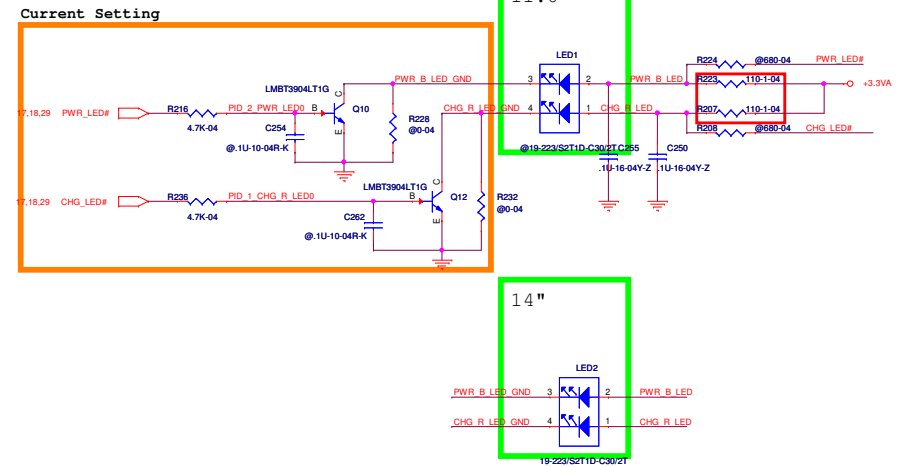
### LED for WIFI & HDD



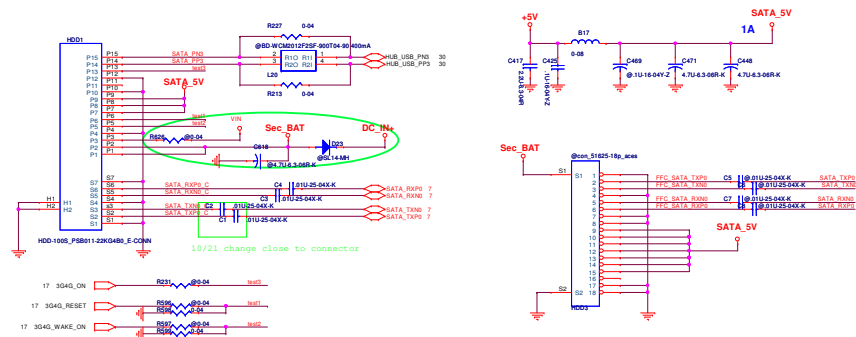
### Power Board(Optional)



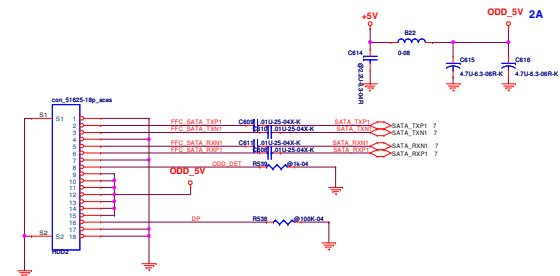
## Charge LED



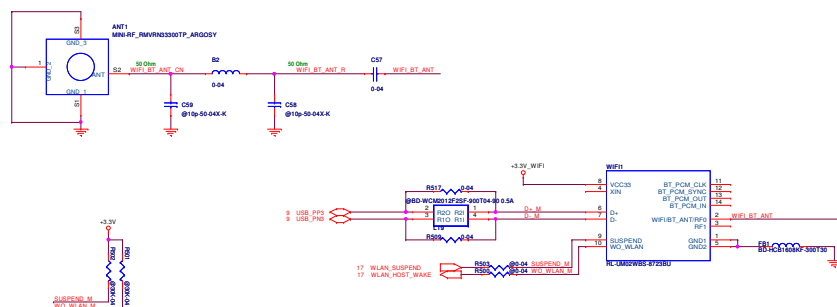
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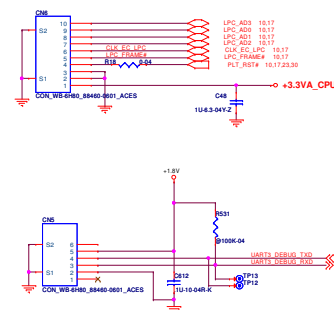
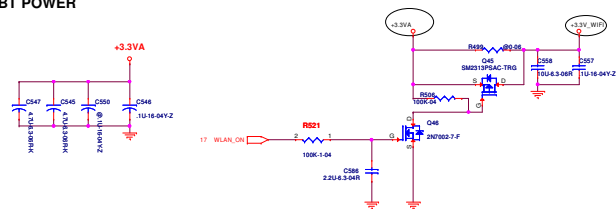
## SATA-ODD



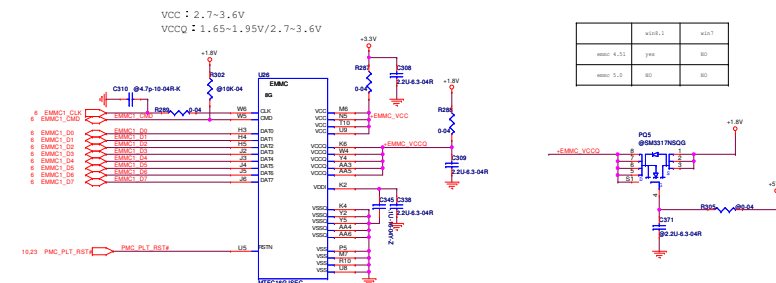
## WIFI/BT 2014/11/26



## DEBUG CN

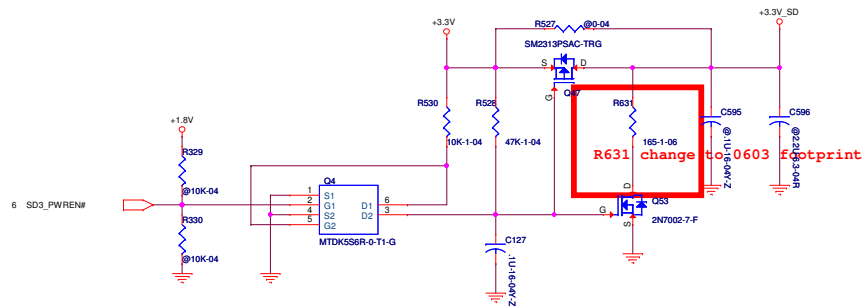
**WIFI/BT POWER**

## EMMC

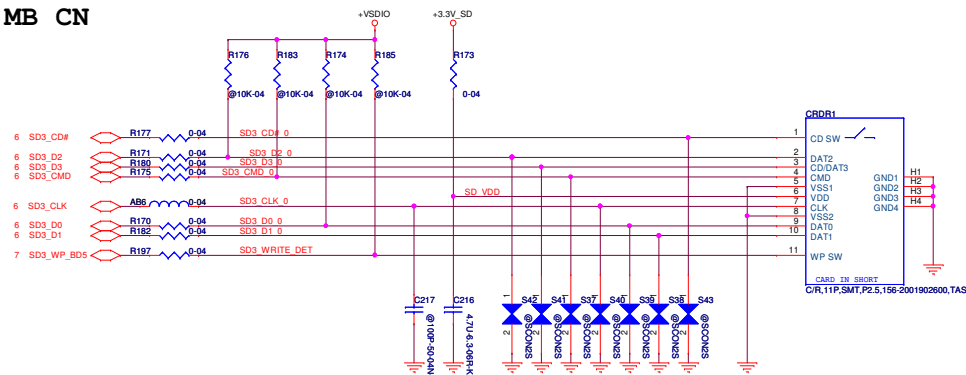


	win0.1	win1
esmc 4.51	yes	NO
esmc 5.0	NO	NO

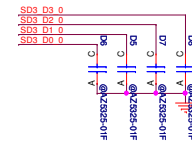
## SD POWER



## SD MB CN

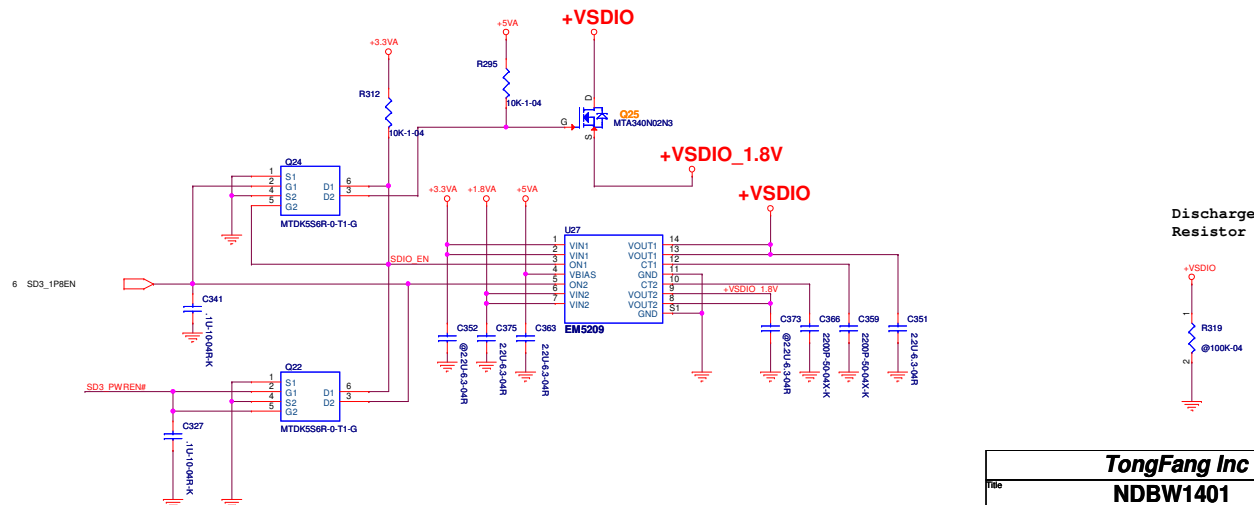


## ESD



## Support Ultra High Speed SD

SD3_1P8EN	High	Low
ON1	Low	Low
	1.8V	3.3V



Discharge Resistor

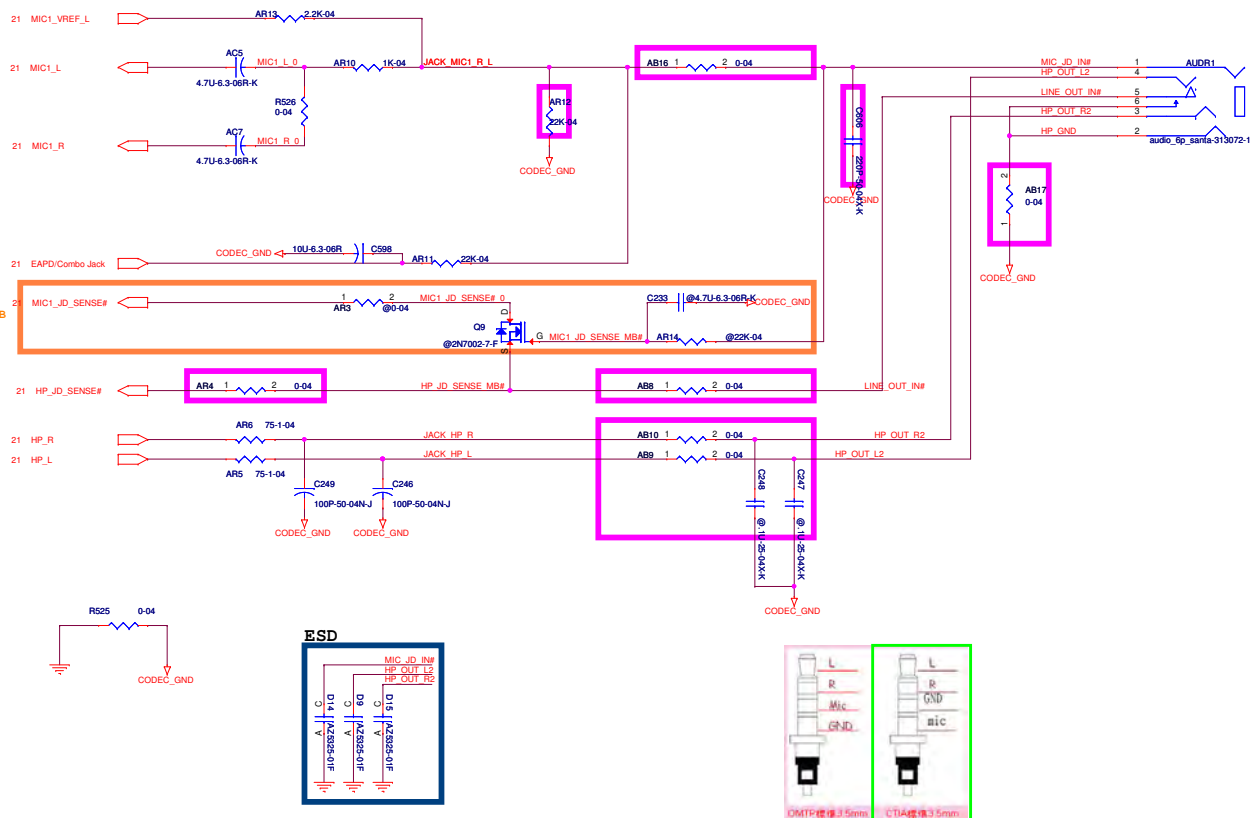
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NDBW1401

Rev	Document Number	Rev
Custom	LAN/CARD READER/15DB/RT8111	B1
Date: Thursday, September 17, 2015	Sheet 20 of 31	

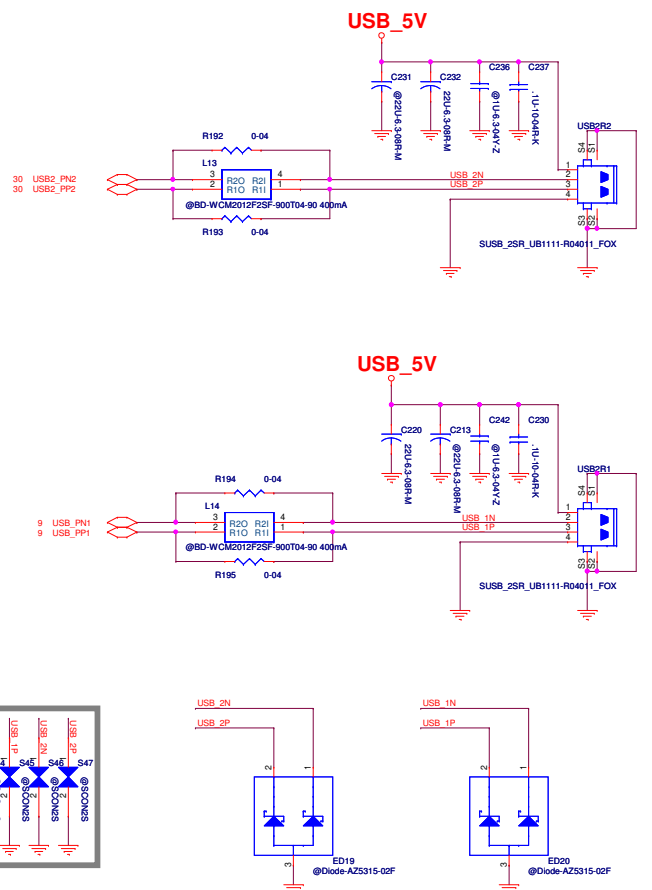


2 IN 1 Audio Jack / USB

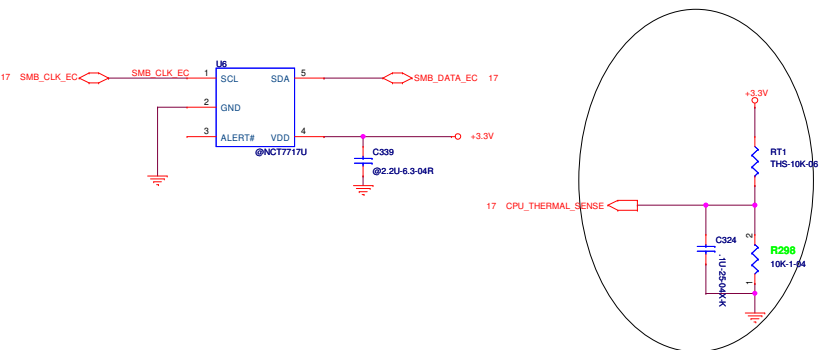
FOR  
ALC2690-VB  
MIC JD



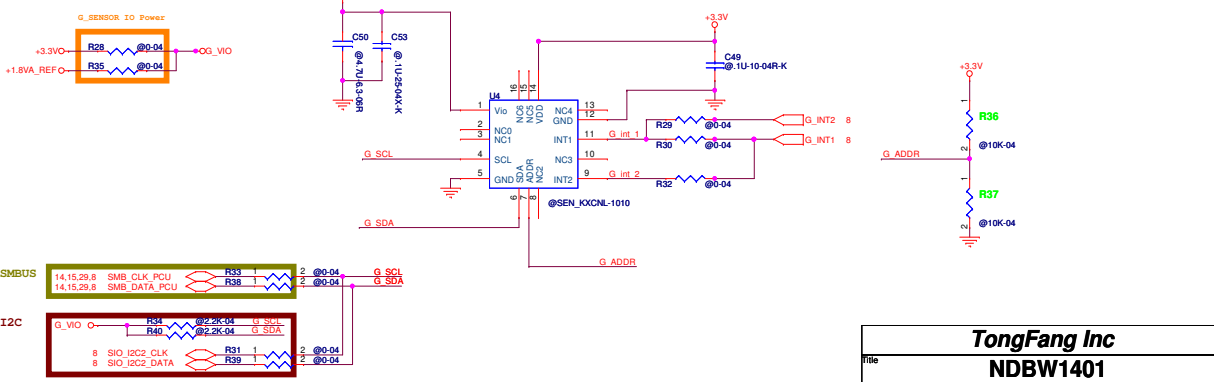
USB2.0



CPU Thermal Sensor

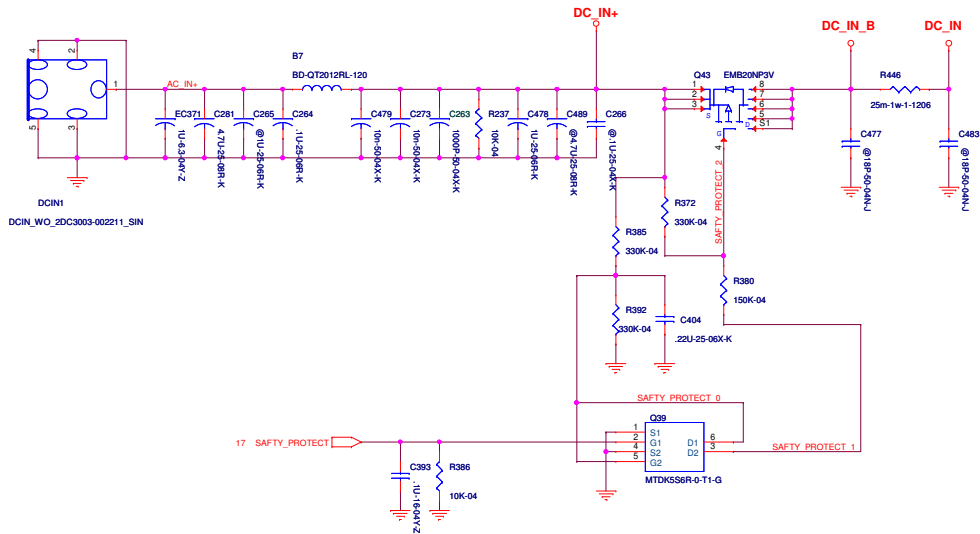


G SENSOR

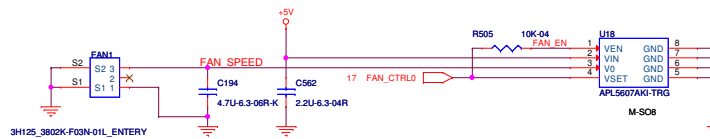


## DC IN

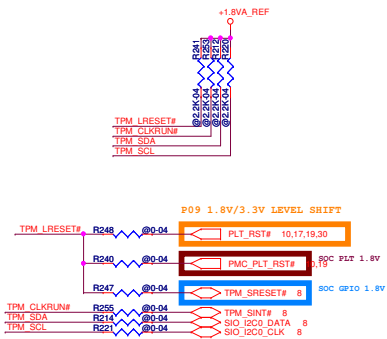
PROJECT	NDBT1401		
Adaptor	40W		
Rsense	25m Ohm		
Stop Charger			



## FAN CONTROLLER



## TPM I2C Interface for NPCT65X 2014/11/18



## Second DC IN

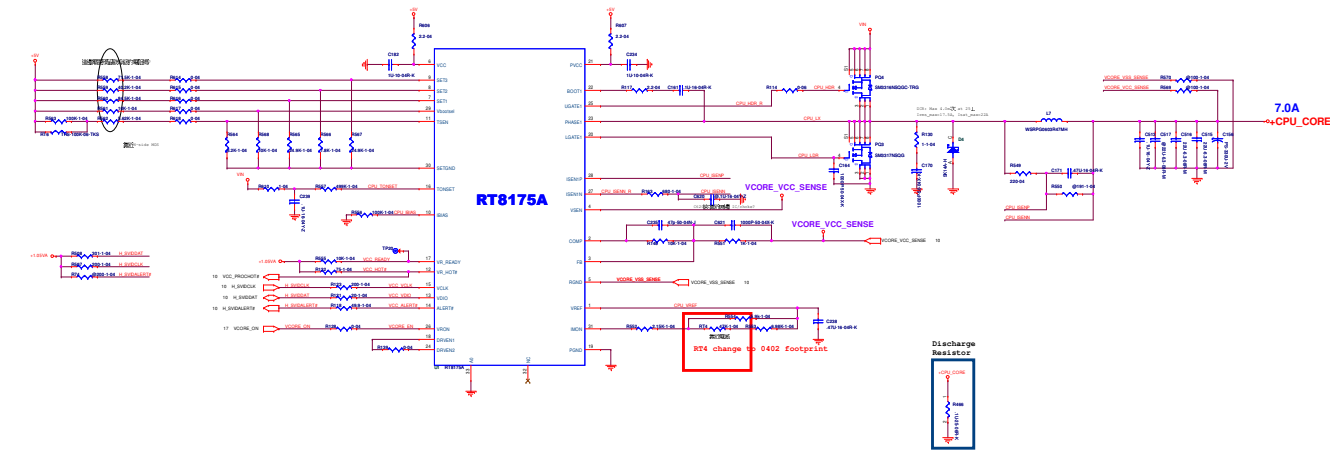




+CPU\_CORE

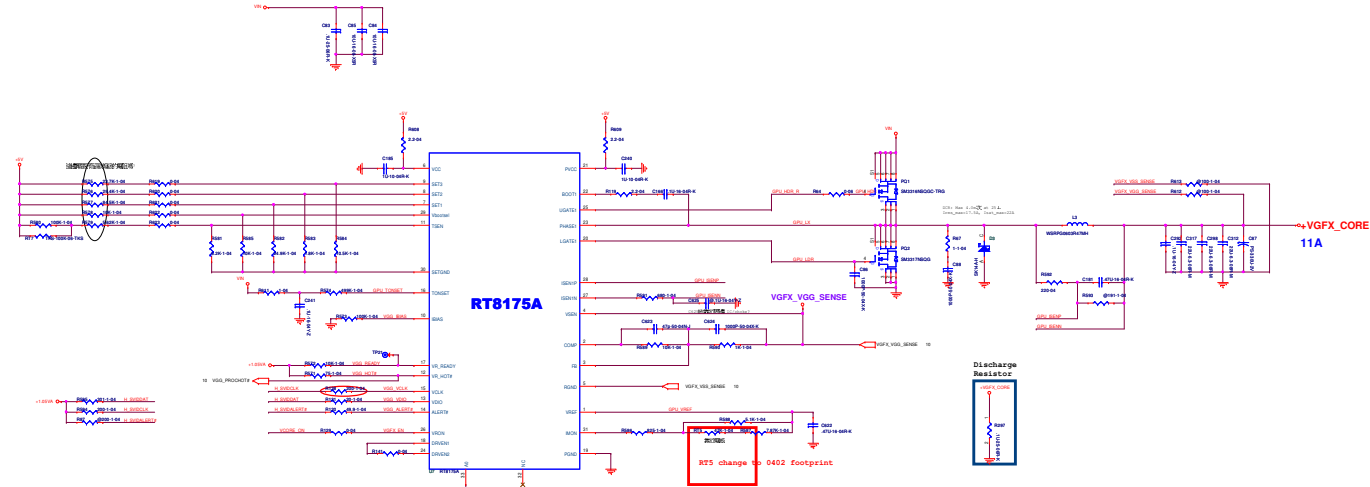
Q51	Q51.0	Q51.0	Q51.0
Q52	Q52.0	Q52.0	Q52.0
Q53	Q53.0	Q53.0	Q53.0

Note: Place RT1 close to inductor on the same side

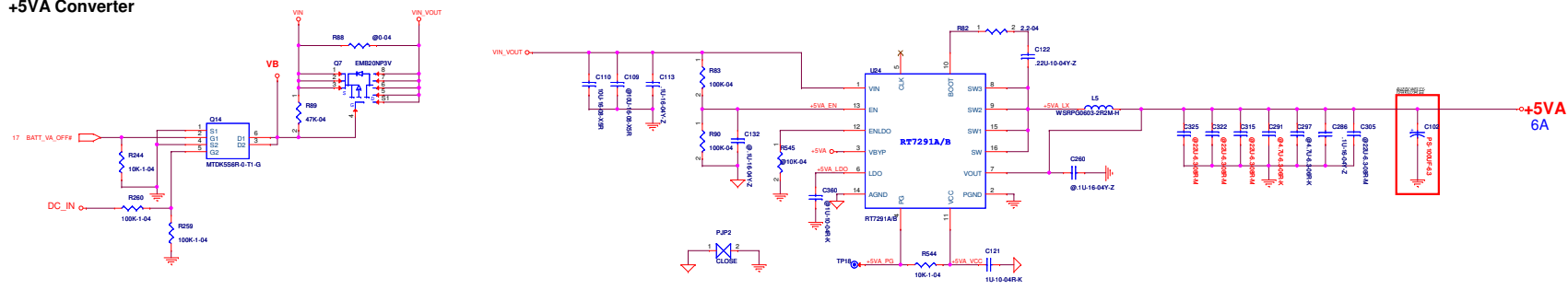


+VGFX\_CORE

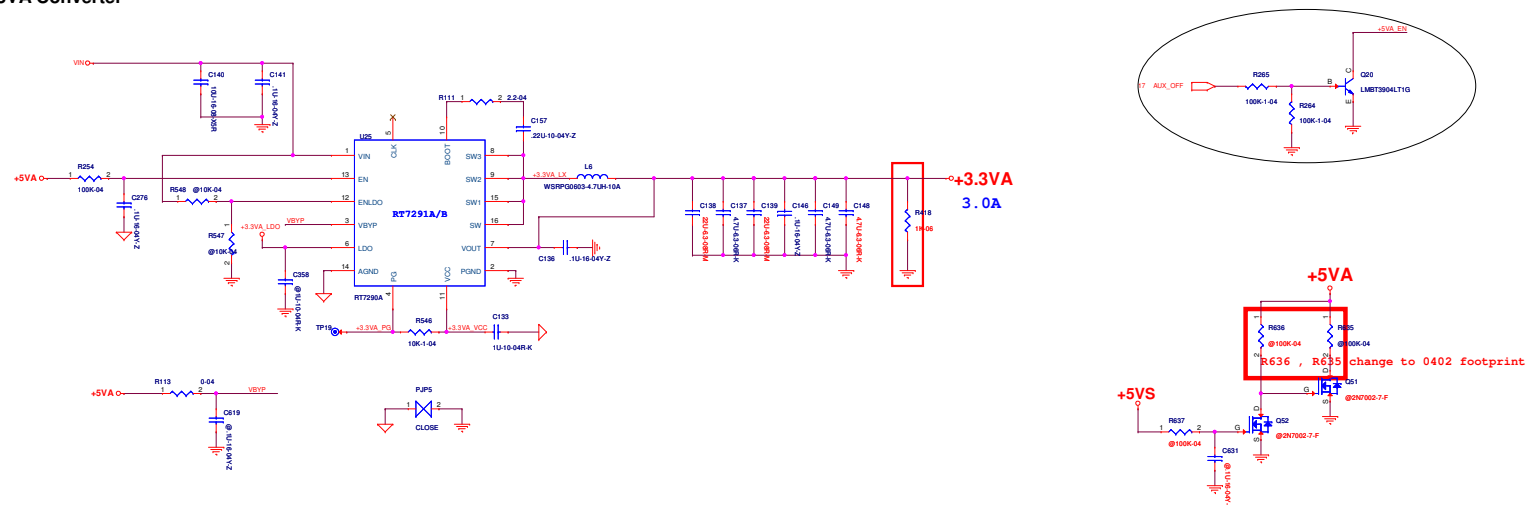
Note: Place RT3 close to inductor on the same side



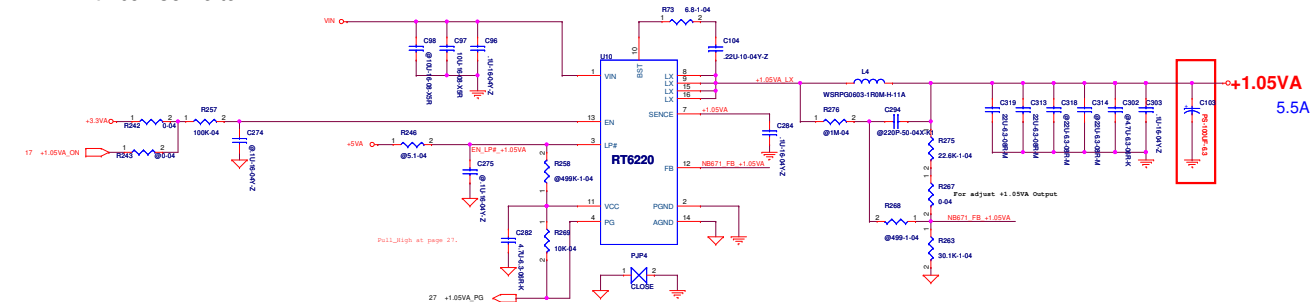
### +5VA Converter



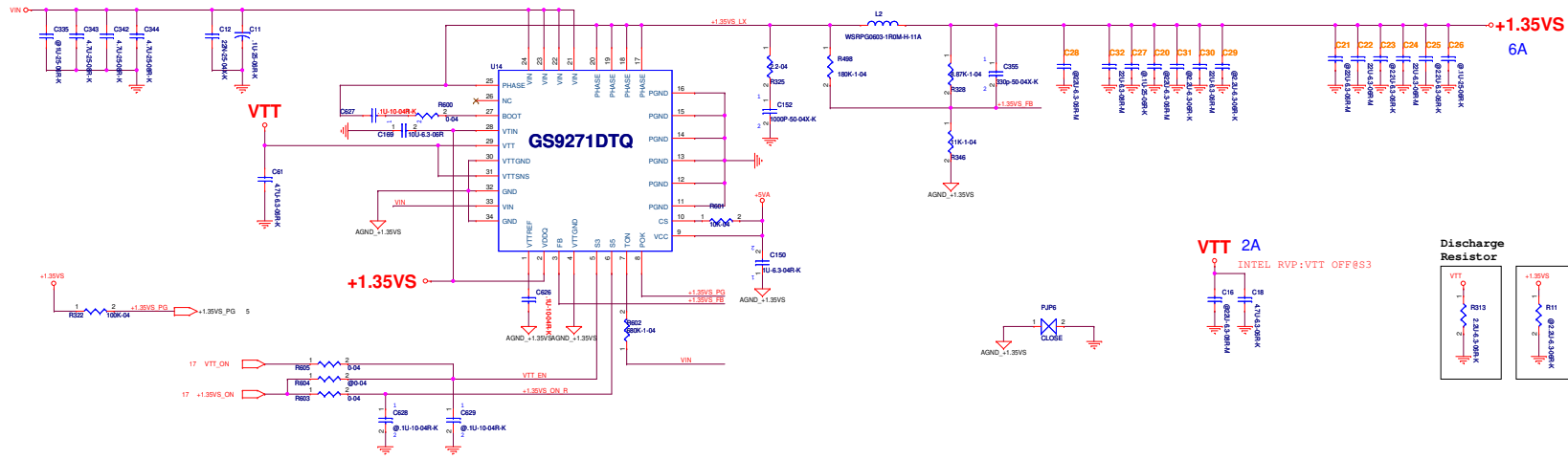
### +3.3VA Converter



### +1.05V Converter

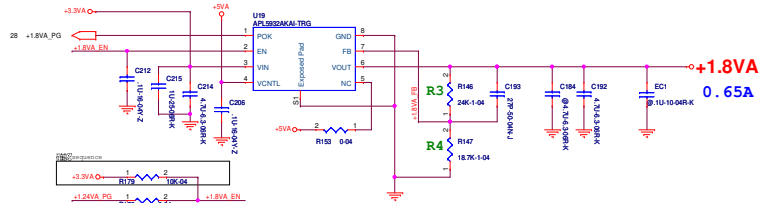


+1.35VS



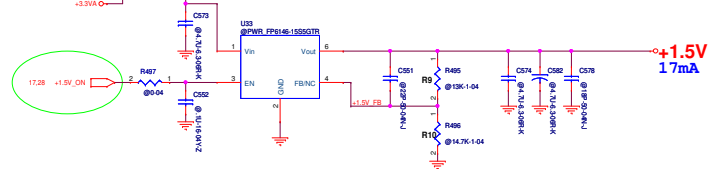
+1.8VA

$V_{OUT} = V_{REF} * (1 + R3/R4)$   
 $0.8 * (1 + 24/18.7) = 1.8267$



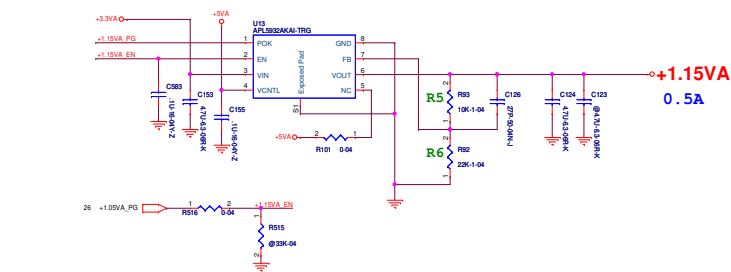
+1.5V

$V_{out} = 0.8V * (1 + R9/R10)$   
 $0.8V * (1 + 13K/14.7K) = 1.5075V$



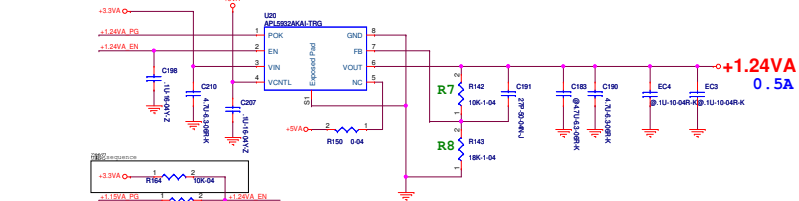
+1.15VA

$V_{OUT} = V_{REF} * (1 + R5/R6)$   
 $0.8 * (1 + 10/22) = 1.164$

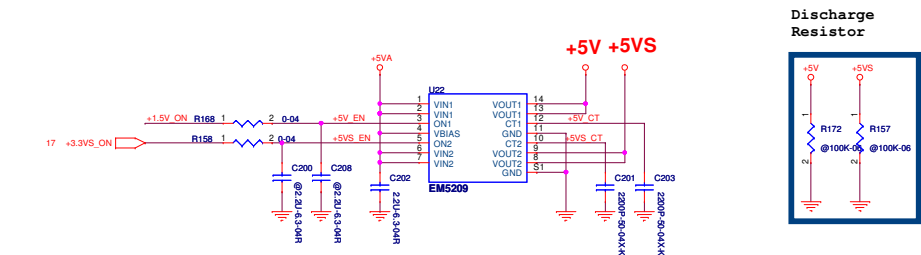


+1.24VA

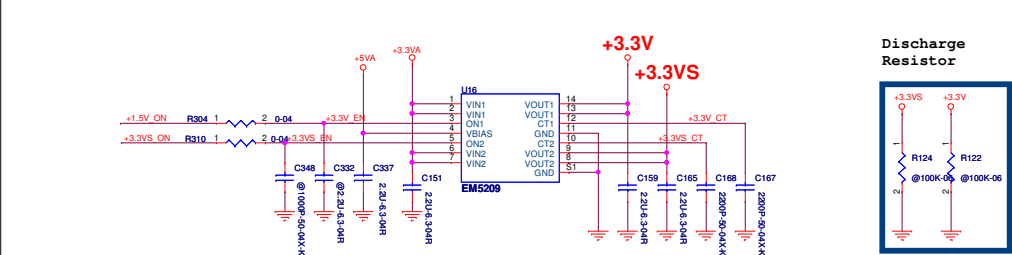
$V_{OUT} = V_{REF} * (1 + R7/R8)$   
 $0.8 * (1 + 10/18) = 1.244$



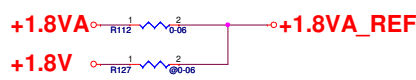
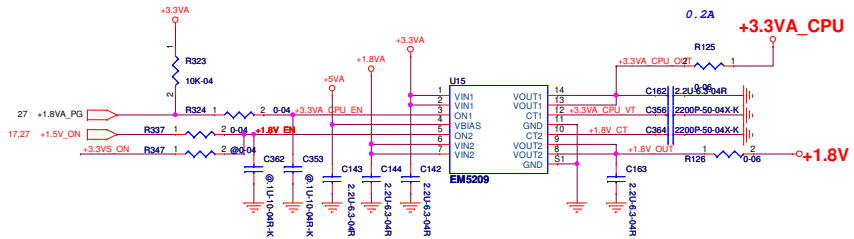
VCCSW +5V/+5VS



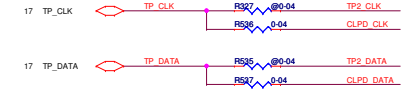
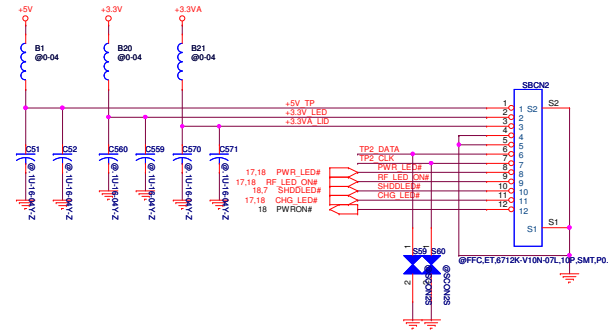
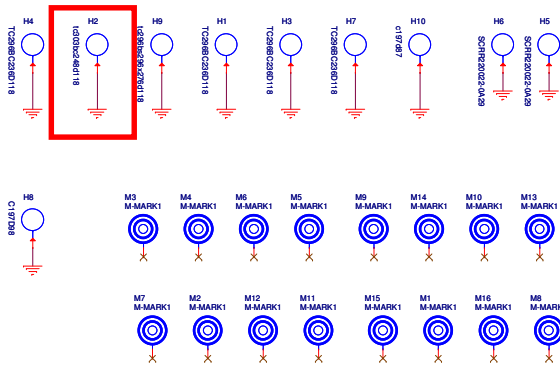
VCCSW +3.3V/+3.3VS



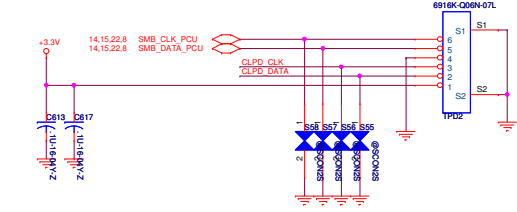
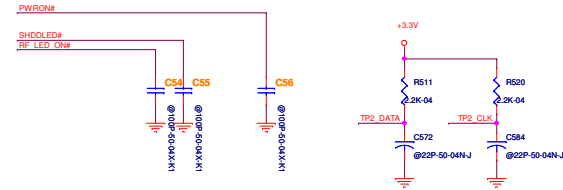
VCCSW +1.8V  
VCCSW +3.3VA\_CPU



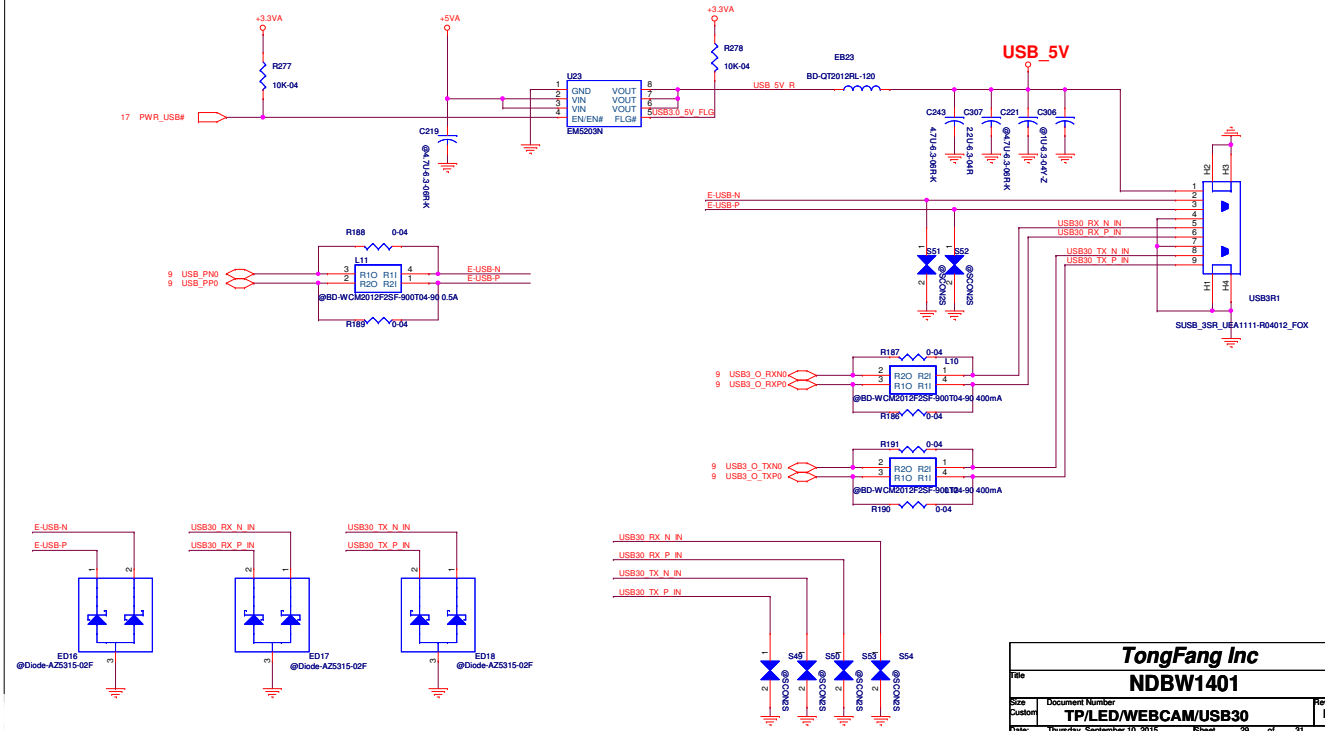
## TP DB Connector

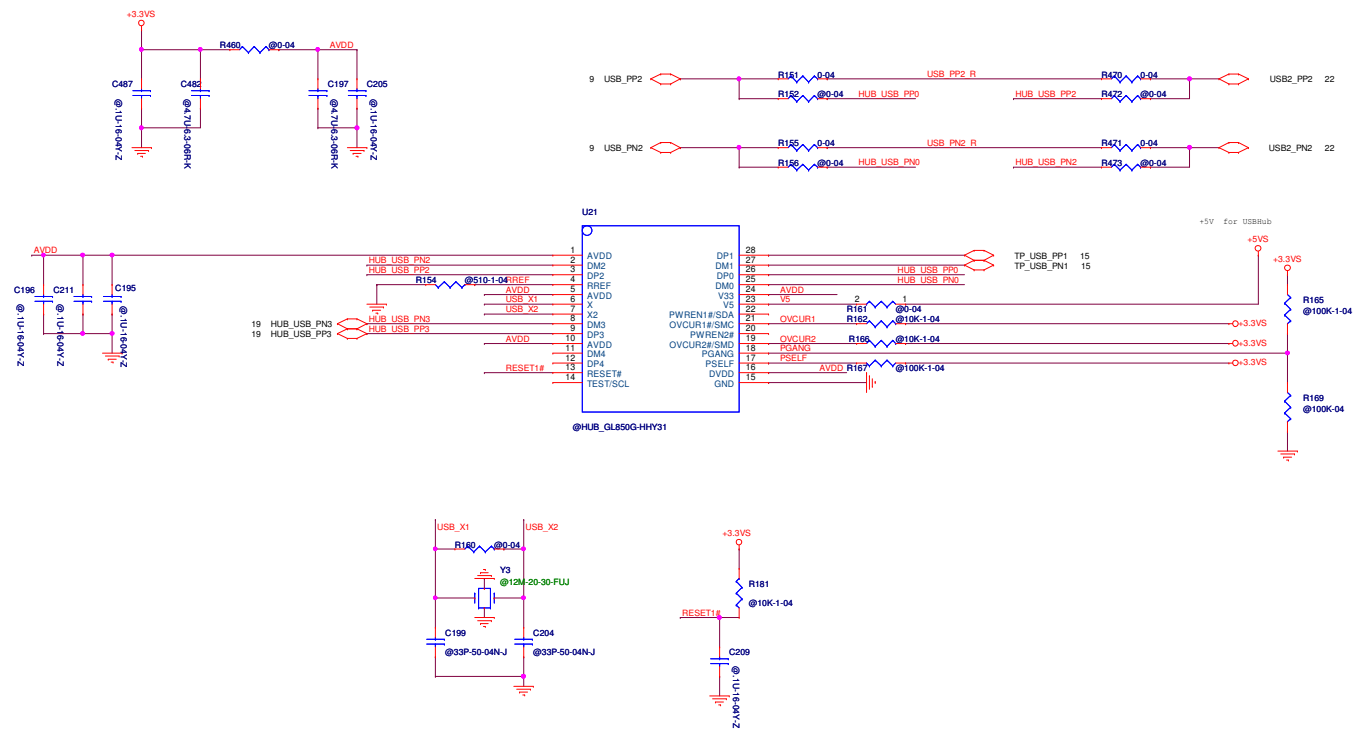


不知道方向 cable 接法 所以無法確認 pin define

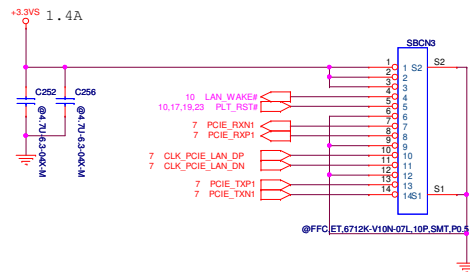


## Enhance USB3.0 Port





LAN(for AIO)



B phase

- 1. ER182, ER183 EMI solution
- 2. R245修改為100 ohm
- 3. 新增VIN\_LCD放電路徑, R233改為100 ohm, 新增Q50
- 4. 修改+1.5V\_PG改為+1.5V\_ON
- 5. R402改為200 ohm, USB2.0 信號才會PASS
- 6. R305刪除
- 7. 新增R498 180K, R328改為8.06K, R346改為10K, C355上件容值改為330p
- 8. +1.05V solution: R276, R268, R258, C294 皆OP
- 9. Vcore, Vgfx新增snuuber R130, R67: 1 ohm, C88, C170: 1000p
- 10. ACZ\_BITCLK新增電容EC160
- 11. VIN\_LCD ESD 元件ED3
- 12. AC\_IN+新增1uF電容EC371
- 13. eMMC VDDQ1預留一組switch(PQ5), 原因是SOC漏電會串到1.8V
- 14. C107, C112修改為27P
- 15. SERIRQ新增level shift (U17, R326, R628, R629, R630, C251, C553)
- 16. TXE\_disable(GPIO\_SUS5)修改
- 17. 新增TXE\_disable(Q32)
- 18. C424, C403, C416改為22uF
- 19. 新增C447, C458, C433, C445 1uF, C632 22uF
- 20. R138改為200 ohm
- 21. EMI要求 (Medion)
- 1uF: C453, C493, C413, C244, C242, C236, C265, C517, C325, C138, C319, C335, C27, C221 共14顆
- 0.1uF: C397, C441, C293, C278, C268, C311, C68, C469, C266, C526, C260, C358, C619, C274, C26, C51, C52, C560, C570, C613, C306 共21顆
- Diode, SMD, GSE0520QFF, GT: ED3, D9, D14, D15
- 22. 調整transient C621, C624 改為1000p, R140, R589改為10K, R551, R590改為1K

B1

- 1. RT4, RT5, R635, R636 0603 footprint change to 0402 footprint
- 2. Del JP
- 3. Change HDD, ODD 18 pin conn pin define
- 4. Change H2 footprint
- 5. Add Q55, Q54, R639, R638, C634, R641 for disable CCD power
- 6. Add Q53, R631 for cardreader

V1.0

- 1. 新增5VA poscap(C102), R418加一顆下地電阻(1K ohm) 刪除MLCC (C325, C322, C315, C291, C286)解高頻音
- 2. 修改CN2 pin define
- 3. OP R641
- 4. Co-lay BX/CX EC, 修改SPEI ROM的power 1.8V
- 5. R534上件, SIRIRO周邊零件OP (U17, R628, R629, R630, C553, R628, C251)
- 6. 新增C103 100uF POSCAP (BurnIn test)
- 7. R402改為150 ohm(USB driving)
- 8. LED R223, R207 改為110 ohm
- 9. CN5, CN6刪除
- 10. VCC, VGG家diode (SK34, 位置: D3, D4)
- 11. +1.05V新增RC (R246, C275)
- 12. C138, C139 改為22uF (0805), C148上件4.7uF 0603
- 13. R78 OP
- 14. B13刪除, B23上件